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| 10/582,377 | 03/29/2007 | Stanton Earl Weaver Jr. | GLOZ 200196US01 | 3872 |

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FAY SHARPE LLP
1228 Euclid Avenue, 5th Floor
The Halle Building
Cleveland, OH 44115

| EXAMINER | |
|---|---|
| CHHAYA, SWAPNEEL | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/582,377 | WEAVER JR. ET AL. | |
| | Examiner | Art Unit | |
| | SWAPNEEL CHHAYA | 2895 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *32-37* are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/9/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Group I, claim(s) 1-31, drawn to light emitting package comprising a chip carrier, a light emitting chip attached to the top surface of the chip carrier.

2. Group II, claim(s) 32-37, drawn to light emitter comprising a chip carrier, lead frame electrically contacting electrodes of the light emitting chip, and a support with printed circuitry

3. The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the second group contains diverging subject matter with regards to the printed circuitry, and the electrodes of the chip carrier.

4. During a telephone conversation with attorney of record on 3/10/2010 a provisional election was made without traverse to prosecute the invention of light emitting package, claims 1-31. Affirmation of this election must be made by applicant in

replying to this Office action. Claims 32-37 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

***Specification***

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 23 states that the chip carrier is soldered to the printed circuit board, the specification states that the chip carrier is soldered to the lead frame, it is unclear as to how a solder connection to the printed circuit board would not be conductive.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 7, 9-11, 15-22, 24-25, 29, 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishinaga et. al. (US Patent 6093940).

1. A light emitting package comprising: a chip carrier having top and bottom principal surfaces;
at least one light emitting chip attached to the top principal surface of the chip carrier; and a lead frame attached to the top principal surface of the chip carrier.(Fig. 1 column 4 lines 10-25)

2. The light emitting package as set forth in claim 1, further
comprising:
an encapsulant encapsulating at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and leads of the lead frame extending outside the encapsulant. (column 4 lines 30-50)

3. The light emitting package as set forth in claim 1, further
comprising:
one or more areas of electrically conductive material disposed on the top principal surface of the chip carrier, the attachment of the lead frame to the top principal surface

electrically contacting the one or more areas of electrically conductive material. (Fig. 1,4,5 column 4 lines 30-50)

4. The light emitting package as set forth in claim 3, wherein the one or more areas of electrically conductive material include:
a first area of electrically conductive material defining a first electrical terminal; a second area of electrically conductive material electrically isolated from the first area, the second area defining a second electrical terminal of opposite electrical polarity from the first electrical terminal; (Fig. 1,4,5 column 4 lines 30-50)
electrodes of the light emitting chip being electrically connected with the first and second electrical terminals; and
the lead frame being attached to the first and second electrical terminals. (Fig. 1,4,5 column 4 lines 30-50 column 5 lines 5-20)

7. The light emitting package as set forth in claim 4, wherein at least one electrode of the light emitting chip is wire bonded to one of the first and second electrical terminals. (Fig. 8)

9. The light emitting package as set forth in claim 3, wherein:
the one or more areas of electrically conductive material include:
a first area of electrically conductive material defining a first electrical terminal,
a second area of electrically conductive material electrically isolated from the first area,

the second area defining a second electrical terminal of opposite electrical polarity from the first electrical terminal, and

a third area of electrically conductive material electrically isolated from the first and second areas of electrically conductive material, the third area of electrically conductive material defining a series interconnection terminal; and the light emitting chip includes first and second light emitting chips, electrodes of the first light emitting chip being electrically connected with the first and series interconnection electrical terminals and electrodes of the second light emitting chip being electrically connected with the second and series interconnection electrical terminals, and the lead frame being attached to the first and second electrical terminals. (Fig. 1,5,8 column 4 lines 30-45 column 5 lines 5-25)

10. The light emitting package as set forth in claim 9, wherein the light emitting chip further includes:

a third light emitting chip, electrodes of the third light emitting chip being electrically connected with the first and series interconnection electrical terminals. (column 4 lines 45-60)

11. The light emitting package as set forth in claim 10, wherein the light emitting chip further includes:

a fourth light emitting chip, electrodes of the fourth light emitting chip

being electrically connected with the second and series interconnection 10 electrical terminals. (column 4 lines 45-60)

15. The light emitting package as set forth in claim 1, wherein the light emitting chip receives electrical power through the lead frame and does not receive electrical power through the bottom principal surface of the chip carrier. (column 6 lines 55-65)

16. The light emitting package as set forth in claim 1, wherein the bottom principal surface of the chip carrier is electrically isolated from the lead frame. (Fig. 6)

17. The light emitting package as set forth in claim 1, wherein the

lead frame has electrical leads extending from portions of the lead frame attached to the top principal surface of the chip carrier, the electrical leads being shaped to include lead portions approximately coplanar with the bottom principal surface of the chip carrier. (Fig. 5-6)

18. The light emitting as set forth in claim 17, wherein the bottom principal surface of the chip carrier is at least one of substantially electrically non-conductive and electrically isolated from the lead frame. (column 4 liens 10-15)

19. The light emitting package as set forth in claim 18, wherein the chip carrier, light emitting chip, and lead frame define a surface mountable unit, the light emitting package further comprising:
printed circuitry, the surface mountable unit being mounted on the printed circuitry with the lead portions approximately coplanar with the bottom principal surface of the chip carrier electrically contacting 'the printed circuitry. (column 6 lines 15-35)

20. The light emitting package as set forth in claim 19, further comprising:
a printed circuit board including the printed circuitry, the bottom principal surface of the chip carrier being in thermal contact with the printed circuit board. (column 5 lines 35-55)

21.
The light emitting package as set forth in claim 19, further comprising:
a printed circuit board on which the printed circuitry is disposed, the bottom principal surface of the chip carrier being in direct contact with the printed circuit board. (Fig. 7 column 5 lines 40-55)

22. The light emitting package as set forth in claim 21, wherein the chip carrier is soldered to the printed circuit board. (Fig. 7 column 5 lines 40-55)

24. The light emitting package as set forth in claim 21, wherein an attachment between the lead portions contacting the printed circuitry is different from an attachment of the bottom principal surface of the chip carrier contacting the printed circuit board. (column 5 lines 40-55)

25. The light emitting package as set forth in claim 21, further
Comprising:
an encapsulant encapsulating at least the light emitting chip and the top principal surface of the chip carrier, the bottom principal surface of the chip carrier and at least the lead portions approximately coplanar with the bottom principal surface of the chip carrier extending outside the encapsulant. (column 6 lines 30-45)

29. The light emitting package as set forth in claim 1, wherein the chip carrier comprises: thermally conductive plastic. (column 1 lines 20-25)

31. The light emitting package as set forth in claim 1, wherein the chip carrier is electrically insulating and the lead frame is electrically conductive. (column 4 lines 10-25, 35-45)

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 6, 8, 26, 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Toda et. al. (US Patent 6184544).

5. Ishinaga discloses the claimed invention except for the light emitting chip is flip chip bonded.

Toda discloses:

The light emitting package as set forth in claim 4, wherein the light emitting chip is flip-chip bonded to the first and second electrical terminals. (Fig. 2 column 3 lines 50-60)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use flip chip bonding as taught by Toda, since Toda states at column 3 lines 15-20 that such a modification would improve emission efficiency of the light emitting device.

6. Toda discloses:

The light emitting package as set forth in claim 4, wherein the light emitting chip is flip-chip bonded to the first and second electrical terminals (Fig. 2)

Ishinaga discloses:

using one of thermosonic bonding, solder, and a conductive epoxy. (column 6 lines 35-45)

8. Ishinaga discloses:

The light emitting package as set forth in claim 7, wherein

another electrode of the light emitting chip is wire bonded to the other one of

the first and second electrical terminals. (column 6 lines 55-65)

26. The light emitting package as set forth in claim 1, wherein the chip carrier comprises:

a semi-insulating silicon wafer. (column 3 lines 50-60)

30. The light emitting package as set forth in claim 1, wherein the chip carrier comprises:

ceramic. (abstract)

5. Claims 23, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Perduijn et. al. (U.S.Patent 6392778).

23.

Ishinaga discloses the claimed invention except for the soldered connection

Perduijn teaches:

The light emitting package as set forth in claim 21, wherein the chip carrier is soldered to the printed circuit board, said soldered connection being thermally conductive but not conducting electrical current when the light emitting chip is operated. (abstract)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use thermally conductive connection as taught by Perduijn, since Perduijn states in the abstract that such a modification would cool the chip.

28. Perduijn teaches:

The light emitting package as set forth in claim 1, wherein the chip carrier comprises: metal having at least the top principal surface coated with an insulating layer. (column 3 lines 60-67)

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga.

27.

The light emitting package as set forth in claim 1, wherein the chip carrier comprises:

electrically conductive silicon having at least the top principal surface coated with an insulating layer.

Ishinaga discloses the claimed invention except for the chip carrier comprising conductive silicon with an insulating layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use whatever material that would suit the characteristics required to optimize the function of the LED chip, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin,* 125 USPQ 416.

7. Claim 12-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishinaga in view of Antle et. al. (U.S.Patent 5914501).

12. Antle discloses the claimed invention except for the use of a zener diode.

Antle discloses:

The light emitting package as set forth in claim 9, further

including:

at least one zener diode electrically connected with at least one of the first and series interconnection electrical terminals, and the second and series interconnection electrical terminals. (abstract)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a zener diode as one of the light emitting elements as taught by Antle, since Antle states in the abstract that such a modification would provide electrical over-stress protection and protect from electrostatic discharge.

13.Antle discloses:

The light emitting package as set forth in claim 3, further

including:

at least one electronic component electrically contacting the one or more areas of electrically conductive material, the at least one electronic component regulating behavior of the at least one light emitting chip. (column 2 lines 1-15)

14. The light emitting package as set forth in claim 13, wherein the at least one electronic component includes:

a zener diode electrically connected in parallel with the light emitting chip to provide electrostatic discharge protection. (abstract, column 1 lines 5-20 column 2 lines 1-15)

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SWAPNEEL CHHAYA whose telephone number is (571)270-1434. The examiner can normally be reached on Monday- Thursday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC

/N. Drew Richards/

Supervisory Patent Examiner, Art Unit 2895